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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 15

Application Number: 09/660,186
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Appellant(s): KWAK, DONG YEUNG

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GROUP 2800

Teresa M. Arroyo
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/24/03.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The statement of the grouping of the claims contained in the brief is incorrect. A correct statement of the grouping of the claims is as follows:

A. Independent claim 2 and its dependent claims 3-7.

B. Independent claim 9 and its dependent claims 10-14, and independent claim 15 and its dependent claims 16-20.

The rejection of claims 2-7, 9-14 and 15-20 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,377,323	ONO et al.	4-2002

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 2 and 4-7 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Ono et al.

In regards to claim 2, Ono et al. show all the elements of the claimed invention in figs. 1-3 and the written description. It is a TFT LCD (thin film transistor liquid crystal display), comprising: a first substrate [SUB1] and a second substrate [SUB2]; a scanning line [GL] on the first substrate; a signal line [DL] formed to cross the scanning line, wherein the signal line does not include an extension pattern; a channel layer [AS]

formed along the signal line [DL] and extended to a portion of the scanning line [GL]; source and drain electrodes [SD1, DL] formed separated on the channel layer [AS] over the scanning line [GL]; a pixel electrode [ITO1] connected to the source electrode [SD1]; and a liquid crystal layer [LC] formed between the first substrate [SUB1] and the second substrate [SUB2].

It is inherent that a pixel electrode connected to the drain electrode because the source and drain electrodes in the liquid crystal display device alternate with each other when the polarities are reversed during operation (col. 4, lines 56-64). Therefore, the source electrode [SD1] becomes the drain electrode and the drain electrode [DL] becomes the source electrode when the polarities are reversed during operation. The drain electrode [SD1] is then parallel to the signal line [DL].

In regards to claim 4, Ono et al. further disclose a gate insulating layer [GI] between the scanning line [GL] and the channel layer [AS].

In regards to claim 5, Ono et al. further disclose an ohmic contact layer [d0] between the source and drain electrodes [DL, SD1] and the channel layer [AS] when the polarities are reversed during operation.

In regards to claim 6, Ono et al. further disclose the source electrode [DL] and the signal line [DL] are formed as a unit when the polarities are reversed during operation.

In regards to claim 7, Ono et al. further disclose the drain electrode [SD1] is overlapped with the scanning line [GL] when the polarities are reversed during operation.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al.

In regards to claims 3, 11, 17, Ono et al. further disclose the channel layer [AS] has a width extended in a direction parallel to the signal line [DL] smaller than a width of an extended portion of the scanning line [GL].

It would have been obvious for the channel layer has a width smaller than a width of the signal line extended in a direction parallel to the scanning line because it depends to the desired resistance of the channel layer.

In regards to claims 3, 11, 17, Ono et al. also disclose the channel layer [AS] has a width smaller than a width of the signal line [DL] and the scanning line [GL] in fig. 2.

In regards to claim 9, Ono et al. disclose a TFT in figs. 1-3 and the written description. It is a TFT LCD, comprising: a first substrate [SUB1] and a second substrate [SUB2]; a plurality of scanning lines [GL] on the first substrate; a gate insulating layer [GI] on a surface inclusive of the scanning lines [GL]; a channel layer [AS] on the gate insulating layer to cross the scanning lines [GL] having a portion extended to a top of each of the scanning lines [GL]; source and drain electrodes [SD1, DL] formed separated on the channel layer [AS] over the scanning lines [GL]; the signal line [DL] does not include an extension pattern; a protection film [PSV1] formed on a

surface inclusive of the signal line [DL]; a pixel electrode [ITO1] connected to the source electrode [SD1] on the protection film; a liquid crystal layer [LC] formed between the first substrate [SUB1] and the second substrate [SUB2].

It is inherent that a pixel electrode connected to the drain electrode because the source and drain electrodes in the liquid crystal display device alternate with each other when the polarities are reversed during operation (col. 4, lines 56-64). Therefore, the source electrode [SD1] becomes the drain electrode and the drain electrode [DL] becomes the source electrode when the polarities are reversed during operation. The signal line [DL] then would form as a unit with the source electrode along the channel layer [AS], which is formed to cross each of the scanning lines [GL] when the polarities are reversed during operation. The pixel electrode [ITO1] would then connect to the drain electrode [SD1] on the protection film [PSV1] and the drain electrode [SD1] is parallel to the signal line [DL].

It would have been obvious for the gate insulating layer on an entire surface inclusive of the scanning lines because it protects the TFTs.

It would have been obvious for the protection film formed on an entire surface inclusive of the signal line because it protects the TFTs .

In regards to claim 10, Ono et al. further disclose the drain electrode [SD1] crosses the scanning line [GL] when the polarities are reversed during operation.

In regards to claim 12, Ono et al. further disclose an ohmic contact layer [d0] between the source and drain electrodes [DL, SD1] and the channel layer when the polarities are reversed during operation.

In regards to claim 13, Ono et al. further disclose the scanning line [GL] has a portion enlarged in the vicinity of the signal line [DL].

In regards to claim 14, Ono et al. further disclose the channel layer [AS] is formed along the signal line [DL] over the scanning line [GL]. It would have been obvious for the channel layer has a width enlarged as much as a width of the scanning line is enlarged because it depends to the desired resistance of the channel layer.

In regards to claim 15, Ono et al. show a TFT in figs. 1-3 and the written description. It is a TFT LCD having a first substrate [SUB1], a second substrate [SUB2], and liquid crystal [LC] sealed between the first and second substrates, comprising: a scanning line [GL] on the first substrate; a gate insulating layer [GI] on the scanning line [GL]; a channel layer [AS] on the gate insulating layer; a signal line [DL] formed to cross the scanning line [GL] to cover a portion of the channel layer [AS], wherein the signal line [DL] does not include an extension pattern.

It is inherent that a pixel electrode connected to the drain electrode because the source and drain electrodes in the liquid crystal display device alternate with each other when the polarities are reversed during operation (col. 4, lines 56-64). Therefore, the source electrode [SD1] becomes the drain electrode and the drain electrode [DL] becomes the source electrode when the polarities are reversed during operation. The drain electrode [SD1] would then form on the channel layer [AS] spaced a distance away from the signal line [DL] in parallel to the signal line [DL]. The protection film [PSV1] would then form on a surface of the first substrate inclusive of the drain

electrode [SD1]; a pixel electrode [ITO1] formed on the protection film connected to the drain electrode [SD1]; and the drain electrode [SD1] is parallel to the signal line [DL].

It would have been obvious for the protection film formed on an entire surface of the first substrate inclusive of the drain electrode because it protects the TFT.

In regards to claim 16, Ono et al. further disclose the channel layer [AS] is formed along the signal line [DL].

In regards to claim 18, Ono et al. further disclose the signal line [DL] serves as a source electrode disposed opposite to the drain electrode [SD1] when the polarities are reversed during operation.

In regards to claim 19, Ono et al. further disclose a gate insulating layer [GI] between the scanning line [GL] and the channel layer [AS].

In regards to claim 20, Ono et al. further disclose an ohmic contact layer [d0] between the source and drain electrodes [DL, SD1] and the channel layer [AS] when the polarities are reversed during operation.

(11) Response to Argument

In response to Appellant's argument in page 5 of the Appeal Brief, it is urged that the cited reference (Ono et al.) does not teach source and drain electrodes formed separated on the channel layer over the scanning line; a pixel electrode connected to the drain electrode; wherein the drain electrode is parallel to the signal line as recited by claim 2. However, as mentioned in the rejection and Ono et al.'s written description (column 4, lines 56-64), the naming of each of source and drain electrodes is essentially determined in accordance with a polarity of a voltage applied between the source and

drain electrodes. The source and drain electrodes in the liquid crystal display device of Ono et al. alternate with each other when the polarities are reversed during operation. Therefore, the source electrode [SD1] of Ono et al. would become the drain electrode and the drain electrode [DL] of Ono et al. would become the source electrode when the polarities of the voltage are reversed during operation. Since the drain electrode is [SD1] and the source electrode is [DL], the drain electrode [SD1] is connected to the pixel electrode [ITO1] now and the source electrode [DL] is a part of the signal line [DL] now. The source electrode [DL] and the drain electrode [SD1] formed separated on the channel layer [AS] and the drain electrode [SD1] is parallel to the signal line [DL].

In response to Appellant's argument in pages 5-6 of the Appeal Brief, it is further urged that the drain electrode of Ono et al. is not over the scanning line, parallel to the signal line, and connected to the pixel electrode. However, it is important to note that the gate electrode [GL] (fig. 3) is a part of the scanning line [GL] (fig. 1) because the gate electrode [GL] is extended from the scanning line [GL]. Therefore, the drain electrode [SD1] is now extended toward and overlaps the scanning line [GL], parallel to the signal line [DL], and connected to the pixel electrode [ITO1].

In response to Appellant's argument in pages 6 and 8 of the Appeal Brief, it is urged that Ono et al. never disclose a TFT LCD device in which $C_{gs,}$ a parasitic capacitance between the scanning line and a drain electrode, has a constant value by overlapping a pattern extended from the drain electrode with the scanning line completely. Since the claimed invention never discloses a TFT LCD device in which C_{gs} is constant by

overlapping a pattern extended from the drain electrode with the scanning line completely, it is not necessary for Ono et al. to show such a structure.

Since Ono et al. show each and every feature of independent claim 2, Ono et al. also show each and every feature of dependent claims 4-7.

In response to Appellant's argument in pages 7-8 of the Appeal Brief, it is urged that Ono et al. does not teach all of the features of the present invention, including features describing the relationship of the drain electrode with other elements. Specifically, it is urged that Ono et al. does not teach a plurality of scanning lines on the first substrate; a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of each of the scanning lines; source and drain electrodes formed separated on the channel layer over the scanning lines; a signal line formed as a unit with the source electrode along the channel layer which is formed to cross the scanning lines, wherein the signal line does not include an extension pattern; a pixel electrode connected to the drain electrode on the protection film; wherein the drain electrode is parallel to the signal line. However, it is important to note that a channel layer [AS] is formed on the gate insulating layer [GI] (figs. 2, 3) and under the signal line [DL] (fig. 2). Ono et al. also disclose the data line (signal line) [DL], the semiconductor layer (channel layer) [AS] and the semiconductor layer [dO] form a stacked structure (col. 5, lines 59-67). The scanning line [GL] is formed on the surface of the substrate [SUB1] (col. 9, lines 10-17). Thus, the channel layer [AS] is formed above the scanning line [GL]. Since the signal line [DL] is a continuous layer formed to cross the scanning lines [GL] in fig. 1 and the signal line [DL], the semiconductor channel layer [AS] and the

semiconductor layer [dO] formed the stacked structure, it is inherent that the channel layer [AS] is formed on the gate insulating layer [GI] to cross the scanning lines [GL] having a portion extended to a top of at least one of the plurality of scanning lines [GL] in fig. 1. Ono et al. further disclose the source electrode [DL] and the drain electrode [SD1] formed separated on the channel layer [AS] over the scanning line [GL]; a signal line [DL] formed as a unit with the source electrode [DL] along the channel layer [AS] which is formed to cross the scanning lines [GL], wherein the signal line [DL] does not include an extension pattern; a pixel electrode [ITO1] connected to the drain electrode [SD1] on the protection film [PSV1]; wherein the drain electrode [SD1] is parallel to the signal line [DL]. Therefore, Ono et al. teach all the major features of the present invention, including features describing the relationship of the drain electrode [SD1] with other elements. Ono et al. further teach a channel layer [AS] on the gate insulating layer [GI] to cross the scanning lines [GL] having a portion extended to a top of at least one of the plurality of scanning lines [GL] as recited by claim 9.

In response to Appellant's argument in pages 7-8 of the Appeal Brief, it is urged that Ono et al. does teach all of the features of the present invention, including features describing the relationship of the drain electrode with other elements. Specifically, it is urged that Ono et al. does not teach a combination of elements including a scanning line on the first substrate; a signal line formed to cross the scanning line to cover a portion of the channel layer, wherein the signal line does not include an extension pattern; a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line; a pixel electrode formed on the protection film

connected to the drain electrode; wherein the drain electrode is parallel to the signal line. However, as clearly mentioned in the rejection and the previously paragraphs, the source and drain electrodes in the liquid crystal display device of Ono et al. alternate with each other when the polarities are reversed during operation. Therefore, the source electrode [SD1] of Ono et al. would become the drain electrode and the drain electrode [DL] of Ono et al. would become the source electrode when the polarities of the voltage are reversed during operation. Therefore, Ono et al. disclose a TFT LCD device includes a combination of elements including a scanning line [GL] on the first substrate [SUB1]; a signal line [DL] formed to cross the scanning line [GL] to cover a portion of the channel layer [AS], wherein the signal line [DL] does not include an extension pattern; a drain electrode [SD1] formed on the channel layer [AS] spaced a distance away from the signal line [DL] in parallel to the signal line [DL]; a pixel electrode [ITO1] formed on the protection film [PSV1] connected to the drain electrode [SD1]; wherein the drain electrode [SD1] is parallel to the signal line [DL]. Therefore, Ono et al. teach all of the major features of the present invention, including features describing the relationship of the drain electrode [SD1] with other elements. Ono et al. further teach a drain electrode [SD1] formed on the channel layer [AS] spaced a distance away from the signal line [DL] in parallel to the signal line [DL] as recited by claim 15.

In response to Appellant's argument in page 8 of the Appeal Brief, it is urged that the reference fails to teach or suggest explicitly or implicitly providing a thin film transistor using the specific features as recited by claims 3 and 9-20. However, as explained in

the rejection and the previous paragraphs, Ono et al. show all the major features of the invention as claimed in independent claims 9 and 15. Since the appellant is silent with regards to the relationship between the width of the channel layer and the width of the signal line in claims 3, 11 and 17, it is believed that it would have been obvious for the channel layer has a width smaller than a width of the signal line because it depends to the desired resistance of the channel layer. Fig. 2 of Ono et al. also disclose the channel layer [AS] also has a width smaller than a width of the scanning line [GL] and the signal line [DL]. Since the appellant is also silent with regards to the gate insulating layer and the protection film in claim 9 and the protection film in claim 15, it is believed that it would have been obvious to have the gate insulating layer and the protection film as claimed in claim 9 and the protection film as claimed in claim 15 because the gate insulating layer and the protection film are conventional electrical insulating means in TFT devices. In regards to claims 10, 12, 13, 16 and 18-20, Ono et al. show all the elements of the claimed invention for each of claims 10, 12, 13, 16 and 18-20. Since the appellant is silent with regards to the claimed feature in claim 14, it is believed that it would have been obvious for the channel layer has a width enlarged as much as a width of the scanning line is enlarged because it depends to the desired resistance of the channel layer.

In response to Appellant's argument in page 9 of the Appeal Brief, it is urged that Ono et al. is not attempting to solve similar problems related to device degradation with the same solution as the Appellant. However, it is the claimed invention that distinguishes the prior art from the invention. Therefore, it is not necessary for Ono et

al. to solve the similar problems related to device degradation that is faced by the appellant. Since the device of Ono et al. can read on the claimed subject matters as claimed in claims 9-20, the device of Ono et al. is similar to the device of the appellant. As explained in the previous paragraphs, the Examiner has established a prima facie case of obviousness with regards to claims 9 and 15 and therefore, the rejection should be sustained. Since claims 9 and 15 are being unpatentable over Ono et al., their dependent claims 10-14 and 16-20 are also unpatentable over Ono et al. because they fall together with their parent claims.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Steven Loke

sl
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